1. (amended) A nonvolatile semiconductor memory device comprising a plurality of memory elements formed in the vicinity of the surface of a substrate, a plurality of word lines for driving the memory elements, and a plurality of bit lines,

each of said plurality of memory elements including:

a semiconductor channel forming region formed in the vicinity of the surface of the substrate,

a source region in contact with the channel forming region in the vicinity of the surface of the substrate,

a drain region in contact with the channel forming region at a position facing the source region in the vicinity of the surface of the substrate,

a gate insulating film, including a tunnel insulating film, formed on said substrate adjacent to the channel forming region,

a top insulating film formed on said gate insulating film;

a conductive gate electrode formed on the top insulating film on the gate insulating film, and

a charge storing means facing said surface of the channel forming region and which is provided in the tunnel insulating film and in the gate insulating film and is planarly dispersed to the other neighbor charge storing means in the gate insulating film;

the gate electrode of the plurality of memory elements being respectively connected to the plurality of word lines;

wherein said gate insulating film formed adjacent to the semiconductor channel forming region comprises a Fowler-Nordheim (FN) type tunneling film which has a FN type tunneling electroconductivity and contains material having a dielectric constant greater than that of silicon oxide.

2. (amended) A nonvolatile semiconductor memory device according to claim 1, wherein the FN type tunneling film comprises any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having an FN tunneling electroconductivity.

3. (amended) A nonvolatile semiconductor memory device according to claim 1, wherein the gate insulating film includes a buffer layer formed between the FN type tunneling film and the channel forming region and suppressing an interface trap level.

4. (twice-amended) A nonvolatile semiconductor memory device according to claim 1, wherein the gate insulating film comprises a Pool-Frenkel (PF) type film including any one of a nitride film, an oxynitridge film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTio_3$) film, having a FN type electroconductivity.

5. (amended) A nonvoltatile semiconductor memory device according to claim 4, wherein the gate insulating film

includes a buffer layer formed between the FN type tunneling film and the PN film.

6. A nonvolatile semiconductor memory device according to claim 1, further comprising:

a pull-up electrode in the vicinity of the gate electrode or a wiring layer connected to the gate electrode, via a dielectric film; and

a pull-up gate bias means for applying a voltage to the pull-up electrode.

7. (previously amended) A nonvolatile semiconductor memory device according to claim 6, wherein

a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines, and

a selected transistor is connected between the pull-up gate bias means and the pull-up electrode, said pull-up gate bias means supplying a voltage having a polarity the same as a polarity of a boosting voltage for boosting the precharged word line by a capacitance coupling.

8. A nonvolatile semiconductor memory device according to claim 6, wherein the pull-up electrode is arranged in the vicinity of an upper portion of the gate electrode or a

connection layer connected to the gate electrode, via the dielectric film.

9. (twice-amended) A nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises a source region contacted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

wherein a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines,

wherein the source region and drain region of each memory transistor are connected to a common line in a bit direction, electrically insulated to and intersecting the word line, and

wherein said nonvolatile semiconductor memory device further comprises

a write inhibit voltage supply means for supplying a reverse-biased voltage to the source region and/or the drain region of the memory transistor the gate electrode of which is connected to the word line selected at a writing, through the common line, to make the source region and/or the drain region in a reverse-biased state to the channel forming region, and

a non-selected word line biasing means for supplying a voltage to a non-selected word line at the writing, a polarity of the voltage being a polarity making the non-selected word line in a reverse biased state to the channel forming region.

10. (previously amended) A nonvolatile semiconductor memory device according to claim 9, wherein the write inhibit voltage supply means supplies the reverse bias voltage to the source region and/or the drain region to make a bias voltage of the memory transistor connected to the selected word line to thereby prevent an erroneous write and/or an erroneous erase.

11. (previously amended) A nonvolatile semiconductor memory device according to claim 9, wherein the non-selected word line biasing means supplies a voltage having a polarity for reverse-biasing to the non-selected word line to make a bias voltage or the memory transistor connected to the non-selected word line to thereby prevent an erroneous write and/or an erroneous erase.

12. (previously amended) A nonvolatile semiconductor memory device according to claim 9, wherein the non-selected word line biasing means biases the gate electrode to the source region so that a voltage of the gate electrode becomes a low level equal or lower than an inhibit gate voltage.

Please add the following new claims:

Please reinstate the original claims 13 to 22.

52. (newly-added) A non volatile memory device according to claim 1 wherein said gate insulating film includes a buffer layer adjacent said tunnel insulating film and said surface of the substrate.

53. (newly-added) A nonvolatile semiconductor memory device according to claim 1 wherein said gate insulating film includes a tunnel insulating film, a nitride film, and said top insulating film in that order sandwiched between said surface of said substrate and said gate electrode, a portion of said gate insulating film overlapping each of said source region and said drain region.

REMARKS

This is a full and timely response to the non-final Official Action mailed September 13, 2001. A Petition to extend the Time for This Response to Within the First Extended Month accompanies this paper. Reexamination and reconsideration in light of the above amendments and the following remarks are courteously requested.

Claims 1 to 12 are pending for examination in this application. As a result of a previous requirement for an election of invention, claims 23 to 27 and 28 to 51 are pending in subsequently-filed divisional applications, Ser. No. 09/828,590 and 09/826,815 respectively. Therefore, these claims